

FT.L-PCIEmini 1.1

Changes 1.0 -> 1.1

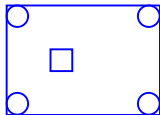
1. Layout: Panel breaking holes added
2. Layout: Vertical spacing in panel: 1.0mm -> 2.0mm
3. Schematics: PCB PN 1.0 -> 1.1
4. Schematics: P2 pin 43 reverse polarity - SATAXPCIE

ZZ1

P/N = 188Z10030

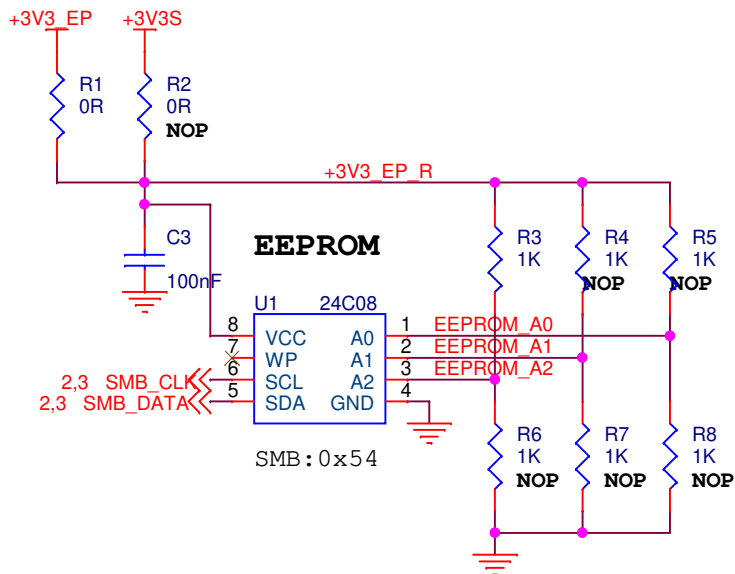
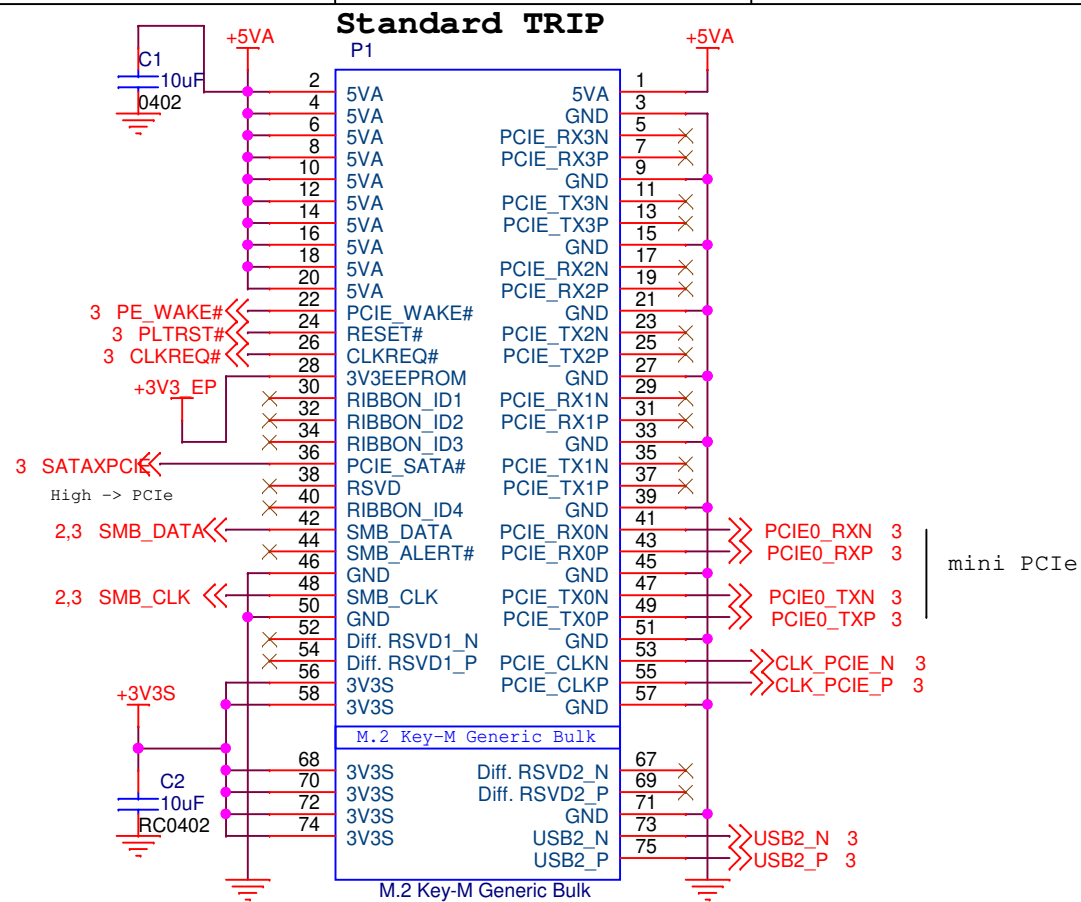
PARSER_VERSION_1.0

PCB1



PCB, FT.L-PCIEmini, Rev 1.1

Title		
01-INDEX		
Size	Document Number	Rev
A	<Doc>	1.1
Date:	Thursday, May 07, 2020	Sheet 1 of 3

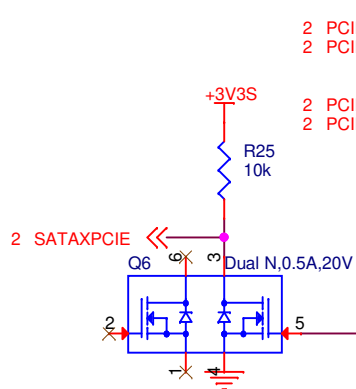


Title 02-TRIP			
Size A	Document Number <Doc>		Rev 1.1
Date:	Thursday, May 07, 2020	Sheet 2 of 3	

The schematic diagram illustrates the Nano-Sim module (U2) and its connections to the SIM PWR, SIM RST, SIM CLK, SIM VPP, and SIM DATA lines. The module is a 10-pin connector with the following pins and connections:

- VCC**: Connected to SIM PWR via capacitor C4 (1uF).
- RST**: Connected to SIM RST via capacitor C5 (33pF).
- CLK**: Connected to SIM CLK via capacitor C8 (33pF).
- VPP**: Connected to SIM VPP via capacitor C9 (68pF).
- GND**: Connected to SIM DATA via capacitor C10 (33pF).
- IO**: Connected to SIM DATA via capacitor C11 (33pF).
- DET_SW**: Connected to DET_SW_L via capacitor C10 (33pF).
- 8x SH**: Connected to SH1 via capacitor C5 (33pF).

The module is labeled "Socket, Nano-Sim, Pin eject, SMT, 10pin".

[illegible]

3.3V , up to 3A

The schematic shows the RT8051B DC-DC converter circuit. The input is +5V, which is filtered by capacitors C21, C22, and C23 (10uF each) and a resistor R16 (1R). The RT8051B IC is configured with PVDD, VDD, V3V3_LX, V3V3_FB, V3V3_COMP, and SHDN/RT pins. The output is regulated to +3V3 and filtered by capacitor C19 (220nF). The circuit includes a 2.2uH inductor (L1) and a 140K feedback resistor (R17). The output is also filtered by capacitors C24, C25, and C26 (10uF each) and a resistor R17 (140K). The output is regulated to +3V3 and filtered by capacitor C19 (220nF).

Date: Thursday, May 07, 2020 Sheet 3 of 3